REMARKS

Claims 1-26 are pending. Claims 1 and 14 have been amended. Figures 1, 3, 6, and 7 have been amended per the Examiner's request. In particular, reference numbers 14-19, 29, 35-37, and 106-119 have been deleted from these figures since these reference numbers are not described in the specification. Editorial revisions have been made to the specification per the Examiner's request. No new matter has been added.

Claim Objections

The specification and claims have been objected to for containing grammatical errors. The Examiner's comments have been considered and appropriate correction has been made.

35 U.S.C. §102 Rejections

Claims 1-3, 11-16, and 24-26 have been rejected under 35 U.S.C. §102(b) as anticipated by Sager et al. (US Patent 5,828,868, hereinafter "Sager").

Claims 2, 3, and 11-13 depend from claim 1. Claim 1 recites a computer system including a high frequency ALU driven by a high clock frequency and a low frequency ALU driven by a low clock frequency, by which low clock frequency a critical path instruction can be executed correctly. If the high frequency ALU of claim 1 can execute an instruction correctly, the execution result of the high frequency ALU is output as an execution result of a pipeline execution stage. However, if the high frequency ALU cannot execute the instruction correctly, the execution result of the low frequency ALU is output as an execution result of the pipeline execution stage instead of the execution result of the high frequency ALU.

Sager discloses a computer system including a latency-intolerant execution sub-core and a latency-tolerant execution core. *See e.g.* column 5, lines 28-43. The execution result of the latency-tolerant core is output, not as an execution result of the pipeline execution stage, but to the latency-intolerant sub-core. *Id.* The execution result of the latency-intolerant sub-core is then output as an execution result of the pipeline execution stage. *Id.*

Sager fails to disclose or suggest a computer system including two ALU's that execute instructions in parallel. Sager further fails to disclose or suggest a computer system including a execution result of the low frequency ALU that is output as an execution result of the pipeline

execution stage instead of the execution result of the high frequency ALU. Even if the latency-intolerant sub-core and the latency-tolerant core can be considered similar to the high frequency and low frequency ALU's of claim 1, a point applicants do not concede, the sub-core and core execute operations in series rather than in parallel. *Id.* Furthermore, the execution result of one is sent to another core for further execution rather than being output independently and exclusively from the execution result of another core. *Id.* Therefore, Sager does not anticipate claim 1. Claims 2, 3, 11-13 are allowable for at least the same reasons.

Claims 15, 16, and 24-26 depend from claim 14. Claim 14 recites a method for controlling a pipeline operation in a computer system including using a high frequency ALU driven by a high clock frequency, a low frequency ALU driven by a low clock frequency, by which low clock frequency the critical path instruction can be executed correctly. Claim 14 further recites outputting the execution result of the high frequency ALU as an execution result of a pipeline execution stage if the high frequency ALU can execute an instruction correctly or outputting the execution result of the low frequency ALU as an execution result of the pipeline execution stage instead of the execution result of the high frequency ALU if the high frequency ALU cannot execute the instruction correctly.

As discussed above with respect to claim 1, the latency-intolerant and latency-tolerant cores disclosed in Sager operate in series rather than in parallel. Furthermore, as discussed above with respect to claim 1, Sager fails to disclose or suggest outputting the execution result of the low frequency ALU as an execution result of the pipeline execution stage instead of the execution result of the high-frequency ALU. Therefore, Sager does not anticipate claim 14 for at least the same reasons as those discussed with respect to claim 1. Claims 15, 16, and 24-26 are allowable for at least the same reasons.

35 U.S.C. §103 Rejections

Claims 4-9, and 17-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sager in view of Kreitzer (US Patent No. 5,253,349, hereinafter "Kreitzer"). This rejection is respectfully traversed. Claims 4-9 depend from claim 1. Claims 17-22 depend from claim 14. Kreitzer does not fix the shortcomings of Sager discussed above.

Claims 10 and 22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Sager in view of Ryan (U.S. Patent No. 4,456,995, hereinafter "Ryan"). This rejection is

respectfully traversed. Claim 10 depends from claim 1. Claim 22 depends from claim 14. Ryan does not fix the shortcomings of Sager discussed above.

In view of the above amendments and remarks, Applicant respectfully requests a Notice of Allowance. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

Respectfully submitted,

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